PATENT APPLICATION

TECHNIQUES FOR REDUCING LEAKAGE CURRENT IN ON-CHIP IMPEDANCE TERMINATION CIRCUITS

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TECHNIQUES FOR REDUCING LEAKAGE CURRENT IN ON-CHIP IMPEDANCE TERMINATION CIRCUITS

BACKGROUND OF THE INVENTION

5   [0001]   The present invention relates to techniques for reducing leakage current, and more particularly, to techniques for reducing leakage current through transistors in an on-chip impedance termination circuit.

[0002]   Integrated circuits have input/output (IO) pins that are used to transmit signals into and out of the circuit. An external termination resistor is usually coupled to each IO pin to

10   provide impedance termination. An impedance termination resistor reduces reflection of input signals on a signal line coupled to an IO pin. Signal reflection causes signal distortion and degrades overall signal quality.

[0003]   The use of external resistors for termination purposes can be cumbersome and costly, especially for integrated circuits that have numerous IO pins. For example, external

15   resistors typically use a substantial amount of board space. As a result, on-chip impedance termination techniques have been developed, because they occupy less board space.

[0004]   Prior art integrated circuits have provided on-chip impedance termination by coupling a field-effect transistor to an IO pin. The gate voltage of the transistor is controlled by a calibration circuit to regulate the impedance of the on-chip transistor. On-chip

20   transistors have also been applied across differential IO pins to provide impedance termination.

[0005]   However, transistors that control on-chip impedance termination circuits can leak unwanted current through their drain/source-to-body diodes even when the transistors are disabled. Therefore, it would be desirable to provide on-chip impedance termination circuits

25   that have reduced leakage current.

BRIEF SUMMARY OF THE INVENTION

[0006]   The present invention provides techniques for reducing the leakage current through on-chip impedance termination circuits. An on-chip impedance termination circuit of the

30   present invention includes a network of resistors and transistors formed on an integrated

circuit. The impedance termination circuit is coupled to one or more IO pins. The transistors can be turned ON and OFF to couple or decouple one or more of the resistors from the IO pins.

[0007] According to the present invention, all of the current paths in the impedance termination circuit are directed through a subset of the transistors (e.g., 2 transistors). The body region of each of the subset of transistors is coupled to a supply voltage to cut off leakage current. By pulling the body regions of these transistors to a supply voltage, their drain/source-to-body diodes are turned OFF to prevent unwanted leakage current. The body connection of the remaining transistors is changed such that junction leakage currents through these transistors are also eliminated.

[0008] Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 illustrates a block diagram of an on-chip impedance termination circuit according to an embodiment of the present invention;

[0010] Figure 2 illustrates a schematic of an on-chip impedance termination circuit that can conduct unwanted leakage current;

[0011] Figure 3 illustrates a schematic of an on-chip impedance termination circuit that prevents unwanted leakage current according to an embodiment of the present invention;

[0012] Figure 4 is a simplified block diagram of a programmable logic device that can implement embodiments of the present invention; and

[0013] Figure 5 is a block diagram of an electronic system that can implement embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] Figure 1 illustrates an on-chip programmable termination impedance circuit 100 according to an embodiment of the present invention. Termination impedance circuit 100 is formed on an integrated circuit such as an application specific integrated circuit (ASIC), a

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programmable logic device (PLD), a field programmable gate array (FPGA), a programmable gate array (PLA), or a configurable logic array.

[0015]   Termination impedance circuit 100 is coupled between two differential input/output (IO) pins INP and INN. IO pins INN and INP are driven by driver circuitry (not shown)
5   between two supply voltage levels. The two supply voltage levels include a high supply voltage, VCC, and a low supply voltage, Ground.

[0016]   Termination impedance circuit 100 provides impedance termination to transmission lines coupled to IO pins INN and INP. Termination impedance circuit 100 can also provide impedance matching to transmission lines coupled to IO pins INN and INP. The impedance
10   of circuit 100 can be set to match the impedance of the transmission lines to reduce signal reflection.

[0017]   Termination impedance circuit 100 includes programmable resistor circuits 110, which are discussed in further detail below. A user of the integrated circuit can program programmable resistor circuits 110 to provide a desired termination resistance value across
15   IO pins INN and INP.

[0018]   Termination impedance circuit 100 also includes common mode driver circuit 111. Common mode driver 111 generates a common mode voltage at node 112. The common mode voltage is in between the high supply voltage VCC and the low supply voltage Ground.

[0019]   An example of impedance termination circuit 100 is illustrated in Figure 2. Figure 2
20   illustrates an on-chip programmable termination circuit 200. Circuit 200 includes field-effect transistors 203, 204, 205, 206, 207, and 208, and resistors 201-202. Circuit 200 is coupled to an IO pin IN. Pin IN can be pin INN or pin INP.

[0020]   N-channel transistor 204 and p-channel transistor 203 form a first pass gate that is controlled by signal BIT1 and its compliment BIT1_B. N-channel transistor 206 and p-
25   channel transistor 205 form a second pass gate that is controlled by signal BIT0 and its compliment BIT0_B. N-channel transistor 208 and p-channel transistor 207 form a third pass gate that is controlled by enable signal EN and its compliment ENB.

[0021]   When transistors 207 and 208 are ON, current flows through resistors 201-202 between pin IN and common mode driver 111. When transistors 203/204 or transistors
30   205/206 are ON, current flows through resistor 201 between pin IN and common mode driver

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111. Turning transistors 203/204 or transistors 205/206 ON provides an alternate current path around resistor 202 that reduces the net resistance of circuit 200.

[0022] Transistors 203-208 are turned OFF to block the flow of current between pin IN and common mode driver 111. However, even when transistors 203-208 are OFF, unwanted leakage current can flow between pin IN and common mode driver 111. The body (i.e., bulk) regions of each of transistors 203-208 are coupled to common mode driver circuit 111.

[0023] When the voltage on pin IN is near supply voltage VCC, unwanted leakage current flows through the drain/source-to-body diodes of p-channel transistors 203, 205, and 207. When the voltage on pin IN is near ground, unwanted leakage current flows through the drain/source-to-body diodes of n-channel transistors 204, 206, and 208. The leakage current causes unnecessary power consumption.

[0024] The leakage current also causes inaccurate termination resistance. For example, if in Figure 1, two of the resistors blocks (110) are turned off using enable signal EN, in order to get a higher termination resistance because fewer blocks 110 are in parallel with each other. However, there can be a leakage current flowing through the body regions of transistors 203-208 in the blocks 110 that are supposed to be shut off. The resistor blocks 110 that are supposed to be shut off are not completely OFF for high input signal swings. That means the resistive paths through those blocks 110 are not actually an open circuit and are contributing to the overall impedance, which causes an inaccurate termination impedance.

[0025] Impedance termination circuits of the present invention block the unwanted leakage current through transistors in programmable termination resistor circuits 110. Figure 3 illustrates an embodiment of an impedance termination circuit 300 of the present invention. Circuit 300 is an example of programmable resistor circuits 110 in Figure 1.

[0026] Circuit 300 includes field-effect transistors 301, 302, 303, 304, 305, 306, and resistors 307-308. N-channel transistor 302 and p-channel transistor 301 form a first pass gate that is controlled by signal BIT1 and its compliment BIT1_B. N-channel transistor 304 and p-channel transistor 303 form a second pass gate that is controlled by signal BIT0 and its compliment BIT0_B. N-channel transistor 306 and p-channel transistor 305 form a third pass gate that is controlled by enable signal EN and its compliment ENB. Signals BIT0, BIT1, BIT0_B, BIT1_B, EN, and ENB can be generated by memory or logic elements on a field programmable gate array. Pass gate 305/306 is turned ON to enable impedance termination circuit 300, and turned OFF to disable circuit 300.

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[0027] Transistors 301-304 are coupled across both terminals of resistor 308 as shown in Figure 3. Therefore, transistors 301-304 cannot bypass the current paths through transistors 305-306. Thus, when transistors 305/306 are both OFF, current flow between pin IN and common mode driver 111 is blocked. When transistors 305/306 are ON, current can flow

5   between pin IN and common mode driver circuit 111.

[0028] Transistors 301-304 are coupled in parallel with resistor 308. One or more of transistors 301-304 can be turned ON to modulate the termination resistance provided by circuit 300.

[0029] The body regions of transistors 305-306 are coupled to a supply voltage as shown in

10   Figure 3. The body of P-channel transistor 305 is coupled to the high supply voltage VCC. The body of N-channel transistor 306 is coupled to ground (the low supply voltage).

[0030] The drain/source-to-body diode (also called the body diode) within p-channel transistor 305 includes a P-N junction between the drain (or source) region and the body region of the transistor. Coupling the N-type body region to VCC prevents the drain/source-

15   to-body diode from becoming forward biased when the voltage at pin IN is near VCC. Therefore, leakage current cannot flow through the drain/source-to-body diode of transistor 305 when transistor 305 is OFF.

[0031] The drain/source-to-body diode within n-channel transistor 306 also includes a P-N junction between the drain (or the source) region and the body region of the transistor.

20   Coupling the P-type body region to ground prevents the drain/source-to-body diode from becoming forward biased when the voltage at pin IN is near ground. Therefore, leakage current cannot flow through the drain/source-to-body diode of transistor 306 when transistor 306 is OFF.

[0032] When transistors 305 and 306 are OFF, current flow between pin IN and common

25   mode driver 111 is completely blocked. No leakage current flows through the channels or the body diodes of transistors 305 and 306.

[0033] According to the present invention, all of the current paths in impedance termination circuit 300 are directed through transistors 305 and 306, and the body diodes of transistors 305-306 are prevented from becoming forward biased. By coupling the body regions of

30   transistors 305-306 to supply voltages VCC and ground, respectively, the body diodes of transistors 305-306 are prevented from conducting leakage current through circuit 300.

[0034]   In Figure 2, the drain/source/body terminals of transistors 203-206 are coupled to common mode driver 111. According to the present invention, the drain/source/body terminals of transistors 301-304 are coupled to node 2 as shown in Figure 3. By coupling the drain/source/body terminals of transistors 301-304 to node 2, leakage current cannot flow through the source/drain/body diodes of transistors 301-304 when these transistors are OFF. This is because Node 2 gets pulled to the same potential as the pin when this resistor is OFF, i.e., when all transistors 301-306 are shut off. With this configuration, the junction voltage across source/body or drain/body diodes of 301-304 is almost zero when the resistor is OFF, which eliminates the junction leakage currents. This was not the case in Figure 2, in which there was leakage through the diode junctions when the resistor was OFF.

[0035]   The present invention provides techniques for blocking leakage current in on-chip impedance termination circuits to reduce power consumption. The body of transistor 305 is pulled up to supply voltage VCC. Circuit 300 substantially reduces the net power consumption by blocking the body diode leakage currents.

[0036]   In Figure 3, each of the impedance termination circuits 110 of Figure 1 can include the circuitry 300 shown in Figure 3. Thus, there are three pass gates 305/306 and three sets of termination resistors 307/308 coupled between common mode driver 111 and pin INP in circuit 100. There are also three pass gates 305/306 and three sets of termination resistors 307/308 coupled between common mode driver 111 and pin INN in circuit 100.

[0037]   Figure 3 illustrates merely one embodiment of the present invention. As will be understood by one of skill in the art, the present invention includes many other embodiments. For example, an impedance termination circuit 110 of the present invention can include one termination resistor. Impedance termination circuit 110 can also include three or more termination resistors. The present invention can also include more pass gates or single transistors that are coupled in parallel with the additional termination resistors.

[0038]   The present invention also includes integrated circuits that have more or less than 6 termination impedance circuits 110. The present invention includes circuits that apply on-chip impedance termination to one pin or to two differential pins.

[0039]   Figure 4 is a simplified partial block diagram of an exemplary high-density PLD/FPGA 400 wherein techniques according to the present invention can be utilized. PLD 400 includes a two-dimensional array of programmable logic array blocks (or LABs) 402 that are interconnected by a network of column and row interconnects of varying length and

speed. LABs 402 include multiple (e.g., 10) logic elements (or LEs), an LE being a small unit of logic that provides for efficient implementation of user defined logic functions.

[0040]   PLD 400 also includes a distributed memory structure including RAM blocks of varying sizes provided throughout the array. The RAM blocks include, for example, 512 bit blocks 404, 4K blocks 406 and a MegaBlock 408 providing 512K bits of RAM. These memory blocks may also include shift registers and FIFO buffers. PLD 400 further includes digital signal processing (DSP) blocks 410 that can implement, for example, multipliers with add or subtract features. I/O elements (IOEs) 412 located, in this example, around the periphery of the device support numerous single-ended and differential I/O standards. It is to be understood that PLD 400 is described herein for illustrative purposes only and that the present invention can be implemented in many different types of PLDs, FPGAs, and the like.

[0041]   While PLDs of the type shown in figure 4 provide many of the resources required to implement system level solutions, the present invention can also benefit systems wherein a PLD is one of several components. Figure 5 shows a block diagram of an exemplary digital system 500, within which the present invention may be embodied. System 500 can be a programmed digital computer system, digital signal processing system, specialized digital switching network, or other processing system. Moreover, such systems may be designed for a wide variety of applications such as telecommunications systems, automotive systems, control systems, consumer electronics, personal computers, Internet communications and networking, and others. Further, system 500 may be provided on a single board, on multiple boards, or within multiple enclosures.

[0042]   System 500 includes a processing unit 502, a memory unit 504 and an I/O unit 506 interconnected together by one or more buses. According to this exemplary embodiment, a programmable logic device (PLD) 508 is embedded in processing unit 502. PLD 508 may serve many different purposes within the system in Figure 5. PLD 508 can, for example, be a logical building block of processing unit 502, supporting its internal and external operations. PLD 508 is programmed to implement the logical functions necessary to carry on its particular role in system operation. PLD 508 may be specially coupled to memory 504 through connection 510 and to I/O unit 506 through connection 512.

[0043]   Processing unit 502 may direct data to an appropriate system component for processing or storage, execute a program stored in memory 504 or receive and transmit data via I/O unit 506, or other similar function. Processing unit 502 can be a central processing

unit (CPU), microprocessor, floating point coprocessor, graphics coprocessor, hardware controller, microcontroller, programmable logic device programmed for use as a controller, network controller, and the like. Furthermore, in many embodiments, there is often no need for a CPU.

[0044]   For example, instead of a CPU, one or more PLDs 508 can control the logical operations of the system. In an embodiment, PLD 508 acts as a reconfigurable processor, which can be reprogrammed as needed to handle a particular computing task. Alternately, programmable logic device 508 may itself include an embedded microprocessor. Memory unit 504 may be a random access memory (RAM), read only memory (ROM), fixed or flexible disk media, PC Card flash disk memory, tape, or any other storage means, or any combination of these storage means.

[0045]   While the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes, and substitutions are intended in the present invention. In some instances, features of the invention can be employed without a corresponding use of other features, without departing from the scope of the invention as set forth. Therefore, many modifications can be made to adapt a particular configuration or method disclosed, without departing from the essential scope and spirit of the present invention. It is intended that the invention not be limited to the particular embodiment disclosed, but that the invention will include all embodiments and equivalents falling within the scope of the claims.

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